PATMOS / VARI 2013
SESSION OVERVIEW

MONDAY, Sept. 9th 2013		TUESDAY, Sept. 10th 2013		WEDNESDAY, Sept. 11th 2013	
8:00-9:00	**Registration**	8:30-9:30	**VARI Industrial Keynote:** Philippe Flatresse & Robin Wilson, ST Microelectronics: System on Chip Variability Reduction, The UTBB FD-SOI Way: Technology and Design Solutions	8:30-9:30	**PATMOS Keynote 2:** Bashir M. Al-Hashimi, University of Southampton, UK: Hardware reliability of embedded systems: are we there yet?
9:00-9:15	**Welcome and Opening**	9:30-9:50	Break	9:30-9:50	Break
9:15-10:15	**PATMOS Keynote 1:** Radu Marculescu, CMU: Design of Future Integrated Systems: A Cyber-physical Systems Approach	9:50-11:15	**PATMOS Session 3:** Microarchitectures and NoCs	9:50-11:15	**PATMOS Session 5:** Simulation and Modeling
10:15-10:30	Break	11:15-11:30	Break	11:15-11:30	Break
10:30-12:45	**PATMOS Session 1:** Sub-Threshold Operation and Variability	11:30-12:45	**PATMOS Session 4:** Circuit Monitoring and Characterization	11:30-12:45	**PATMOS Session 6:** Dynamic Voltage and Frequency Scaling
12:45-14:00	Lunch	12:45-14:00	Lunch	12:45-14:00	Lunch
14:00-15:30	**PATMOS Special Session 1:** Towards Cross Abstraction Level Power Closure	14:00-15:30	**VARI Session 1:** Variability and Aging at Device and Circuit Level	14:00-15:30	**PATMOS Special Session 2:** Low Power Design Methods in Emerging Technologies
15:30-16:00	Break & Posters	15:30-16:00	Break & Posters	15:30-16:00	Break & Posters
16:00-18:15	**PATMOS Session 2:** System-level Power and Thermal Management	16:00-17:30	**VARI Session 2:** Sensors, Tools and design	16:00-17:30	**VARI Session 3:** Variability and Aging Aware Design
				17:30	**Closing Remarks**

19:00	**Social Event** (Gastdozentenhaus)

PATMOS / VARI 2013
DAY 1

PATMOS / VARI Program for Monday, Sept. 9th 2013

9:15-10:15 (Monday): PATMOS Keynote 1

Chair: Jörg Henkel, KIT

Title: Design of Future Integrated Systems: A Cyber-physical Systems Approach

Speaker: Radu Marculescu, Carnegie Mellon University, USA

Abstract: In this talk, we address some fundamental issues related to the modeling and optimization of power and performance of next generation of integrated systems while taking a cyber-physical approach. As such, the focus of the design methodology is not only on establishing a reliable communication infrastructure between the computational elements, but also on including time, communication, and feedback-based control as intrinsic components of the programming model; this goal allows us generalize the classical computational paradigm such that more direct interaction between the cyber-system and physical world becomes possible. Starting from these overarching ideas, we argue that the complex requirements for high-performance and low-power design, as well as reliable and safe operation of future integrated systems call for a truly multidisciplinary approach which brings together concepts and techniques from real-time computing and signal processing, multiprocessor architecture and OS design, as well as distributed and self-organized control.

Bio: Radu Marculescu is a Professor in the Dept. of Electrical and Computer Engineering at Carnegie Mellon University, USA. He received his Ph.D. in Electrical Engineering from the University of Southern California in 1998. He has received the Donald O. Pederson Best Paper Award from the IEEE Transactions of Computer-Aided Design of Integrated circuits and Systems in 2012, the Best Paper Award of IEEE Transactions on VLSI Systems in 2011 and 2005, as well as several best paper awards in major conferences in the area of design automation and multi-core design. Dr. Marculescu is currently an Associate Editor of IEEE Trans. on Computers, IEEE Trans. on Computer-Aided Design of Circuits and Integrated Systems, ACM Trans. on Embedded Computing Systems, and Elsevier Journal of Nano Communication Networks. He has been involved in organizing several international symposia, conferences, workshops, and tutorials, as well as guest editor of special issues in archival journals and magazines. His research focuses on design methodologies and software tools for embedded systems, cyber-physical systems, and biological systems. Radu Marculescu is an IEEE Fellow and an ACM Distinguished Speaker.

PATMOS / VARI 2013
DAY 1

10:30-12:45 (Monday): PATMOS Session 1: Sub-Threshold Operation and Variability

Chair: Lars Bauer, KIT

10:30 **Maximizing Yield in Near-threshold Computing under the Presence of Process Variation**
Nathaniel Conos, Saro Meguerdichian, Sheng Wei, Miodrag Potkonjak, University of California, Los Angeles, USA

10:55 **Ultra Low-Power Standard Cell Design using Planar Bulk CMOS in Subthreshold Operation**
Marc Pons, Jean-Luc Nagel, Daniel Séverac, Marc Morgan, Daniel Sigg, Pierre-François Rüedi, Christian Piguet, CSEM SA, Switzerland

11:20 **Empirical Verification of Fault Models for FPGAs Operating in the Subcritical Voltage Region**
Alex Aa. Birklykke, Peter Koch, Ramjee Prasad, Aalborg University, Denmark
Lars Alminde, GomSpace APS, Denmark
Yannick Le Moullec, Aalborg University, Denmark

11:45 **Variability analysis of Self-Timed SRAM robustness**
Frank Burns, Abdullah Baz, Delong Shang, Alex Yakovlev, School of Electrical and Electronic Engineering, Newcastle University, UK

12:10 **A Variation Tolerant Architecture for Ultra Low Power Multi-processor Cluster**
Daniele Bortolotti, Davide Rossi, Andrea Bartolini, Luca Benini, University of Bologna, Italy

12:35 **A learning tool MOSFET model - A stepping-stone from the square-law model to BSIM4** (Short)
Kjell Jeppson, Chalmers University of Technology, Sweden

14:00-15:30 (Monday): PATMOS Special Session 1: Towards Cross Abstraction Level Power Closure

The Semantic of the Power Intent Format UPF: Consistent Power Modelling from System Level to Implementation
Juergen Karmann, Wolfgang Ecker, Infineon Technologies AG, Germany

Enabling Energy-Aware Design Decisions for Behavioural Descriptions Containing Black-Box IP-Components
Lars Kosmann, Daniel Lorenz, Axel Reimer, OFFIS, Germany
Wolfgang Nebel, Universität Oldenburg, Germany

Power Contracts: A Formal Way Towards Power-Closure?!
Gregor Nitsche, Kim Gruettner, Wolfgang Nebel, OFFIS, Germany

Formal System-on-Chip Verification: An Operation-Based Methodology and its Perspectives in Low Power Design
Joakim Urdahl, Shrinidhi Udupi, Dominik Stoffel, Wolfgang Kunz, University of Kaiserslautern, Germany

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DAY 1

15:30-16:00 (Monday): Break and Poster session

Note: all 7 posters will be presented in all 3 poster sessions, i.e. 15:30-16:00 on Monday, Tuesday, and Wednesday.

Power Consumption Analysis Using Multi-View Modeling
Carlos Gomez, Université Nice-Sophia Antipolis / INRIA, France,
Julien Deantoni, UNS - I3S - INRIA Sophia Antipolis Mediterranee, France,
Frederic Mallet, Universite Nice Sophia-Antipolis, France

A Fully Standard-Cell Delay Measurement Circuit for Timing Variability Detection
Alessandro Sassone, Massimo Petricca, Massimo Poncino and Enrico Macii, Politecnico di Torino, Italy

Automatic Implementation of Low-Complexity QC-LDPC Encoders
Georgios Tzimpragos, Athens Information Technology and National Technical University of Athens, Greece,
Christoforos Kachris, Athens Information Technology,
Dimitrios Soudris, National Technical University of Athens, Greece,
Ioannis Tomkos, Athens Information Technology, Greece

High Level Transforms to reduce Energy Consumption of Signal and Image Processing Operators
Haixiong Ye, ST Microelectronics, France,
Lionel Lacassagne, Joel Falcou, Daniel Etiemble, LRI Univ. Paris-Sud, France,
Laurent Cabaret, Ecole Centrale, France,
Olivier Florente, ST Microelectronics, France

Peak Power Demand Analysis and Reduction by Using Battery Buffers for Monotonic Controllers
Waqaas Munawar, Jian-Jia Chen, Karlsruhe Institute of Technology, Germany

Design Methodology for Low-Power Embedded Microprocessors
Andrea Manuzzato, Fabio Campi, STMicroelectronics, Italy,
Valentino Liberali, Universita' degli studi di Milano,
Davide Pandini, STMicroelectronics, Italy

A Framework with Temperature-Aware Accuracy Levels for Battery Modeling from Datasheets
Massimo Petricca, Alberto Bocca, Donghwa Shin, Alberto Macii, Enrico Macii and Massimo Poncino, Politecnico di Torino, Italy

PATMOS / VARI 2013
DAY 1

16:00-18:15 (Monday): PATMOS Session 2: System-level Power and Thermal Management

Chair: Domenik Helms, OFFIS

16:00 **Optimizing the Configuration and Control of a Novel Human-Powered Energy Harvesting System ***
Vishwa Goudar, Zhi Ren, Paul Brochu, Miodrag Potkonjak, Qibing Pei, University of California, Los Angeles, USA

16:25 **Power saving policies for multipurpose WBAN**
Filippo Casamassima, Elisabetta Farella Luca Benini, University of Bologna, Italy

16:50 **Applying of Quality of Experience to System Optimisation**
Sascha Bischoff, Electronics and Computer Science, University of Southampton, UK,
Andreas Hansson, ARM Ltd, UK,
Bashir M. Al-Hashimi, Electronics and Computer Science, University of Southampton, UK

17:15 **On-line Thermal Emulation: How to speed-up your thermal controller design**
Francesco Beneventi, Andrea Bartolini Luca Benini, University of Bologna, Italy

17:40 **Evaluating the Impact of Substrate on Power Integrity in Automotive Microcontrollers**
Marco Cazzaniga, Universita' degli studi di Milano / STMicroelectronics, Italy,
Patrice Joubert Doriol, STMicroelectronics, Italy,
Emmanuel Blanc, Apache Design Inc., France
Valentino Liberali, Universita' degli studi di Milano, Italy,
Davide Pandini, STMicroelectronics, Italy

18:05 **An Assessment of Software Lifecycle Energy** (Short)
Vasily Moshnyaga, Fukuoka University, Japan

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PATMOS / VARI 2013
DAY 2

PATMOS / VARI Program for Tuesday, Sept. 10th 2013

8:30-9:30 (Tuesday): VARI Industrial Keynote

Chair: Francesc Moll, UPC

Title: System on Chip Variability Reduction, The UTBB FD-SOI Way: Technology and Design Solutions

Speakers: Philippe Flatresse & Robin Wilson, ST Microelectronics, Crolles, France

Abstract: Continued scaling of planar BULK-CMOS technologies enables density increase, but shows diminishing improvements in performance and power dissipation caused by variability and leakage current issues. Having identified that conventional planar bulk CMOS would not meet all the requirements of mobile and consumer multimedia System-on-Chip (SoC) ICs in the coming years, there is consensus in the industry that the next CMOS generations will be based on thin silicon film technologies. In this context, STMicroelectronics has chosen the 2D planar UTBB FD-SOI solution as mainstream CMOS technology, being a natural evolution of the conventional planar Bulk technology. UTBB FD-SOI offers the advantage to strongly reduce the impact of the two major detractors to the efficiency of traditional technology that are the transistor variability and the electrostatics. Thus, Planar UTBB FDSOI technology appears as the most attractive process against variability in SOCs at 28nm and beyond, making it a real differentiator in terms of design simplicity and flexibility. This talk will review how the variability is greatly improved thanks to UTBB FDSOI technology and the associated SOC design solutions.

Bio: Philippe Flatresse received M.S. degree in Electrical Engineering in 1995 and PhD degree in Microelectronics in 1999 from Grenoble Institute of technology. In year 2000, he joined STMicroelectronics Central R&D to deploy the SOI digital design. His current research interests are the convergence of high performance and low standby power towards multimedia mobile applications thru disruptive digital and analog aware design. He has authored or coauthored more than 40 technical papers, and has filed more than 10 patents in advanced CMOS technologies.

Bio: Robin WILSON (IEEE-M'91) received the B.Eng. degree in electrical engineering from the University College Cork, Cork, Ireland, in 1987. From 1987 to 1990, he worked within the semicustom development department of Plessey Semiconductors, UK. In 1990, he joined STMicroelectronics Central Research and Development Department, Crolles, France, where he is currently a design department manager of the Central CAD and Design Solutions Group in the area of high performance energy efficient design. His research interests include high performance design and silicon qualification in advanced CMOS processes.

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DAY 2

9:50-11:15 (Tuesday): PATMOS Session 3: Microarchitectures and NoCs

Chair: Wolfgang Karl, KIT

9:50 **Design of Variable Latency Adder Based On Present and Transitional States Prediction**
Xinghua Yang, Fei Qiao, Chang Liu, Huazhong Yang, Institute of Circuits and Systems, Dept. of Electronic, Engineering, Tsinghua National Laboratory for Information Science and Technology, Tsinghua University, China

10:15 **SET Propagation in Micropipelines ***
Thomas Polzer, Andreas Steininger, Vienna University of Technology, Austria

10:40 **Evaluation of Hop Count Advantages of Network-Coded 2D-Mesh NoCs**
Michael Vonbun, Stefan Wallentowitz, Michael Feilen, Walter Stechele, Andreas Herkersdorf, Technische Universität München, Germany

11:05 **Compiling for Performance and Power Efficiency** (Short)
Ewerton Lima, Brazil; Tiago Xavier, Anderson Faustino Da Silva, Linnyer Ruiz; State University of Maringá

11:30-12:45 (Tuesday): PATMOS Session 4: Circuit Monitoring and Characterization

Chair: Jian-Jia, Chen, KIT

11:30 **Reliability Monitoring of Digital Circuits by in situ Timing Measurement**
Nasim Pour Aryan, Institute for Technical Electronics, Technische Universitaet Muenchen; Germany,
Georg Georgakos, Infineon Technologies AG, Germany,
Doris Schmitt-Landsiedel, Institute for Technical Electronics, Technische Universitaet Muenchen, Germany

11:55 **A Single Built-in Sensor to Check Pull-up and Pull-down CMOS Networks against Transient Faults**
Rodrigo Possamai Bastos, TIMA Lab (CNRS - Grenoble INP - UJF), France,
Frank Sill Torres, DEE, UFMG, Brazil
Jean-Max Dutertre, Ecole des Mines de Saint-Etienne, France,
Marie-Lise Flottes, Giorgio Di Natale, LIRMM, France,
Bruno Rouzeyre, LIRMM. Univ. Montpellier 2, France

12:20 **Metastability Characterization for Muller C-Elements ***
Thomas Polzer, Andreas Steininger, Vienna University of Technology, Austria

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DAY 2

14:00-15:30 (Tuesday): VARI Session 1: Variability and Aging at Device and Circuit Level

Chair: Nadine Azemar, LIRMM

14:00 Keynote: Time-dependent variability in advanced CMOS technologies: from nanoscale mechanisms to circuit level assessment

Speaker: *Montserrat Nafria, UAB*

Abstract: In ultra-scaled devices, because of the aging mechanisms that can be triggered during the device operation, the process-related variability turns into a time-dependent variability, so that the device electrical behavior must be described by statistically distributed parameters that evolve with time. Device aging depends on its particular operation in the IC (i.e., circuit topology, voltages, frequency, duty cycle, temperature…), so that it must be evaluated in a circuital context. Moreover, device time-dependent variability translates into shifts of the circuit parameters, leading to a loss of circuit performance and/or reliability. To establish the link between device aging and circuit operation/performance, statistical circuit simulation, which considers device aging (and also the initial variability), will be needed to capture the time-dependent device/circuit parameter variations. Therefore, a combination of Monte Carlo (to account for variability) and SPICE simulations (to consider the particular circuit configuration and device stress conditions) seems the most suitable approach. In this simulation methodology, the description of the device time-dependent variability is actually the clue for accurate simulations. Therefore, physics-based models of the aging phenomena, whose parameters account for the underlying fabrication technology and operation dependences, are required.

This work is focussed on the most important aging mechanisms in MOSFETs, i.e., Bias Temperature Instabilities (BTI), Channel Hot Carrier (CHC) degradation and Time Dependent Dielectric Breakdown (TDDB), using a multilevel approach, starting at the nanoscale and ending at circuit level. The atomic-scale origin of the different aging mechanisms will be discussed and their most important effects on the device electrical behaviour described, together with examples of physical models for the aging. Emphasis will be done on the electrical characterization of device aging for model parameter extraction. How the effects of process variability, BTI aging and TDDB effects at device level can be considered (with the aid of the physical models) during circuit simulation will be shown, by describing the main features of RELAB, an example of statistical circuit simulation tool. Some circuit simulation examples will show that such kind of tool can be used to identify the weakest devices in a circuit and to evaluate the circuit performance degradation, so that it could be used by circuit designers for circuit performance and reliability improvement, early during the design phase of the circuit.

Bio: Montserrat Nafria received the Ph.D. degree in Physics from the Universitat Autonoma de Barcelona, Spain, in 1993, where she is currently a Full Professor at the Department of Electronic Engineering. Her major research interests include CMOS device and circuit reliability. Currently, she is working on the characterization and modelling of the aging (BTI and channel hot carrier degradations) and variability of advanced MOS de-

vices. This is done from the nanoscale level, by studying the phenomena using Atomic Force Microscope-related techniques, up to circuit level, by developing device models for circuit simulators that account for their time-dependent variability. She is also interested in the characterization and modelling of Resistive-Switching devices. She is the author or coauthor of more than 200 research papers in scientific journals and conferences in all these fields.

14:30 Measurements of process variability in 40nm regular and non-regular layouts
J. Mauricio, F. Moll, S. Gómez, UPC

14:50 Process variation compensation for PLL on FDSOI 28nm
A. Fonseca, E. De Foucauld, P. Lorenzini, G. Jaquemod, CEA-LETI, EPIB-UNS

15:10 Yield Estimation Model using a Lithography Hotspot Classifier
S. Gómez, F. Moll, UPC

15:30-16:00 (Tuesday): Break and Poster session

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16:00-17:30 (Tuesday): VARI Session 2: Sensors, Tools and design

Chair: Marc Belleville, CEA LETI

16:00 Keynote: Statistical learning for test and control of analog/RF circuits

Speaker: ***Salvador Mir, TIMA***

Abstract: The increasing variability of process parameters in nanometric CMOS integrated circuits is a major concern for design and test engineers. Circuit output parameters, including both specified performances and other test measurements, suffer also an increasing variability that affects device yield and test quality. Statistical techniques have been traditionally used for modeling parameter variability at the design stage and to estimate circuit yield. Today, statistical techniques aimed at modeling the complex relationships between circuit parameters are being proposed in the research community to address tasks such as the design of alternative built-in test techniques and the control of analog/RF circuits. In this talk, we will illustrate the use of probability density estimation, machine learning and parameter identification to assist design and test engineers for test and control tasks.

Bio: Salvador Mir has an Industrial Engineering (Electrical, 1987) degree from the Polytechnic University of Catalonia, Barcelona, Spain, and M.Sc. (1989) and Ph.D. (1993) degrees in Computer Science from the University of Manchester, UK. He is a Research Director of CNRS (Centre National de la Recherche Scientifique) at TIMA Laboratory in Grenoble, France. He is currently Vice-director of TIMA and he is leading the RMS (Reliable

Mixed-signal Systems) Group. He has published many papers in the field of mixed-signal/RF/MEMS test and he is co-author of two books on silicon Microsystems.

16:30 Characterization of MOSFET Local Systematic Variability in Presence of Statistical Variability
O. Jonani, F. Piliado, G. Castaneda, A. Juge, STMicoelectronics, IMEP_LAHC

16:50 Temperature and Fast Voltage On-Chip Monitoring using Low-Cost Digital Sensors
L. Vincent, P. Maurine, E. Baigné, S. Lesecq, J. Mottin, CEA-LETI, LIRMM

17:10 Robust Design of Microwave Circuits by Iterative Algorithm Using Orthogonal Arrays
T. Nakagawa, T. Kirikoshi, Mitsubishi Electric Corporation

PATMOS / VARI 2013
DAY 3

PATMOS / VARI Program for Wednesday, Sept. 11th 2013

8:30-9:30 (Wednesday): PATMOS Keynote 2

Chair: Alex Yakovlev, U. Newcastle

Title: Hardware reliability of embedded systems: are we there yet?

Speaker: Bashir M. Al-Hashimi, University of Southampton, UK

Abstract: The last ten years has seen major academic research efforts to improve the reliability of embedded systems in the presence of various hardware faults. The talk will review the highlights of this research and also report on some effective industrial practices in dependable hardware design. The aim is to motivate further focused research in system-level design approach and automation tools for reliable and energy-efficient design of future many-core embedded systems.

Bio: Bashir M. Al-Hashimi holds the endowment ARM chair in Computer Engineering, school of Electronics and Computer Science (ECS), University of Southampton, UK. He is the director of the Pervasive Systems Centre for multidisciplinary research in Electronics and Computer Science, and he is a co-director of the ARM-ECS research centre. He serves as Dean of Research, Faculty of Physical Sciences and Engineering.

He has recently (2013) been elected Fellow of the Royal Academy of Engineering for his contribution to low-power design and test of mobile computing systems; fellows of the Academy comprise the UK most eminent and distinguished engineers and are recognised for their excellence in the science and practice of engineering. In 2009, he was elected fellow of the IEEE for significant contributions to design and test of low-power circuits and systems.

Prof. Al-Hashimi has published 300 papers, authored or co-authored 5 books, and graduated 32 PhD students. He served as Technical Programme chair and General Chair of DATE conference in 2009 and 2011, respectively.

Home Page: http://www.ecs.soton.ac.uk/~bmah

9:50-11:15 (Wednesday): PATMOS Session 5: Simulation and Modeling

Chair: Jörg Keller, Fernuniversität Hagen

9:50 **Efficient Power Intent Validation Using Loosely-Timed Simulation Models**
Fabian Mischkalla, Wolfgang Mueller, University of Paderborn, Germany

10:15 **Modeling Noise Correlations for Model-Based Switch-Capacitor Sigma-Delta ADCs Design Optimization**
Fu-Chuang Chen, Sheng Tzu-En, NCTU, Taiwan

10:40 **An Efficient Eye-Diagram Determination Technique for Multi-Coupled Interconnect Lines**
Junghyun Lee, Yungseon Eo, Hanyang University, Korea

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11:05 **Accurate and Fast Power Annotated Simulation, Application to a Many-Core Architecture** (Short)
Thomas Ducroux, Germain Haugou, Vincent Risson, STMicroelectronics, France,
Pascal Vivet, CEA-Leti, France

11:30-12:45 (Wednesday): PATMOS Session 6: Dynamic Voltage and Frequency Scaling

Chair: Jose Monteiro, TU Lisbon

11:30 **Methodology for Power Mode Selection in FD-SOI circuits with DVFS and Dynamic Body Biasing**
Yeter Akgul, Diego Puschini, Suzanne Lesecq, Edith Beigne, CEA/LETI/DACLE/LIALP, France,
Pascal Benoit, Lionel Torres, LIRMM, France

11:55 **Coupled Voltage and Frequency Control for DVFS Management**
Mauricio Altieri, Warody Lombardi, CEA Grenoble, Minatec Campus, France,
Diego Puschini, Suzanne Lesecq, CEA/LETI/DACLE/LIALP, France

12:20 **Crown Scheduling: Energy-Efficient Resource Allocation, Mapping and Discrete Frequency Scaling for Collections of Malleable Streaming Tasks ***
Christoph Kessler, Nicolas Melot, Linköping University, Sweden,
Patrick Eitschberger, Jörg Keller, Fernuniversität in Hagen, Germany

14:00-15:30 (Wednesday): PATMOS Special Session 2: Low Power Design Methods in Emerging Technologies

Power Modeling and Characterization of Graphene-Based Logic Gates
Massimo Poncino, Politecnico di Torino

Dynamic Electrothermal Macromodeling Techniques for Thermal-Aware Design of Circuits and Systems
Alessandro Magnani, Vincenzo d'Alessandro, Niccolò Rinaldi, Massimiliano de Magistris, University of Napoli, Italy
Klaus Aufinger, Infineon Technologies AG, Germany

Power/Performance Implications of NoC Microarchitecture Decisions for Multicore Systems with Dynamic Frequency Scaling
Davide Zoni, Politecnico di Milano, Italy
José Flich, Universitat Politècnica de València, Spain,
William Fornaciari, Politecnico di Milano, Italy

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PATMOS / VARI 2013
DAY 3

15:30-16:00 (Wednesday): Break and Poster session

Note: all 7 posters will be presented in all 3 poster sessions, i.e. 15:30-16:00 on Monday, Tuesday, and Wednesday. For details about the posters, see program on Monday.

16:00-17:30 (Wednesday): VARI Session 3: Variability and Aging Aware Design

Chair: Antonio Rubio, UPC

16:00 **Reconfiguration Proactive Techniques for Process and Aging Variation Aware Cache Design**
P. Peyman, A. Rubio, UPC

16:20 **An Energy Efficient Pulse-Triggered Flip-Flop Robust to Local Variations in Ultra Low Voltage**
S. Bernard, A. Valentian, D. Bol, J. Legat, M. Belleville, CEA-LETI, ICTEAM

16:40 **A Design for Yield approach for redundant FLASH ADC**
H.Y. Darweesh, G. Leger, A. Rueda, IMS-CSIC

17:00 **Sizing for Static Noise Margins Revisited**
M. Tache, V. Beiu, W. Ibrahim, F. Khasbash, M. Alioto, United Arb Emirates University, Intel Labs