PATMOS 2013

23rd International Workshop on
Power and Timing Modeling, Optimization and Simulation

September 9 – 11, 2013
Karlsruhe, Germany
http://www.itiv.kit.edu/patmos-vari2013/

Call for Papers

Submission Deadline: June, 7th 2013

About PATMOS

PATMOS 2013 is co-located with VARI 2013 in Karlsruhe, Germany. PATMOS has a history of more than 20 years and it was one of the first conferences world-wide to focus on low power. For further information, the official 2013 PATMOS web page is here: http://www.itiv.kit.edu/patmos-vari2013/

The Scope of PATMOS 2013: ICT Energy-Efficiency

The traditional scope of the PATMOS conference series has mainly been about and around the design of circuits and architectures optimized for highest performance at lowest power consumption. But meanwhile, power-efficiency has become extremely important for many more areas spreading far beyond this traditional R&D niche.
Energy-efficient ICT (Information and Communication Technology) infrastructures are a key issue of local and global economies. Some predict that until the year 2030, if current trends continue, the electricity consumption caused by the Internet to grow by up to 30 times. Energy prices will grow substantially. The next generation of oil and gas seismic simulations, for instance, will require orders of magnitude more computational power. Already during the past 11 years the price of crude oil increased by a factor of 9 with significantly increasing tendency in the future. The strong increase of wireless communication and the growth of cloud computing will further contribute to this trend.
A future peta- or exa-flop supercomputer would need its own power plant if the gap between computation and power consumption could not be resolved: At the Top 500 list from 2008 through 2012 the energy efficiency has improved from 228 MFlops/Watt to 280 MFlops/Watt, yielding only an average factor of 1.05 per year. But not only for data centers and future supercomputers electricity is often the largest cost factor.
Compared to the current status of research on power-efficient high performance ICT we are facing the challenge to achieve results being better by several orders of magnitude.

It is the intention of PATMOS 2013 to think beyond current solutions such that the very wide gap between computation and the massive energy consumption for ICT infrastructures can be closed.

Important Dates:

Submission deadline (Regular Papers):	**June 07, 2013**
Submission deadline (Special Sessions etc.):	**June 15, 2013**
Notification of acceptance:	**July 25, 2013**
Camera-ready papers due:	**August 15, 2013**
PATMOS/VARI Conference:	**September 9-11, 2013**

Organization:

Program Co-Chairs

Jörg Henkel, KIT, Germany,
henkel@kit.edu

Alex Yakovlev, Newcastle University, UK
alex.yakovlev@newcastle.ac.uk

General Co-Chairs:

Jürgen Becker, KIT, Germany,
becker@kit.edu

Reiner Hartenstein, TU Kaiserslautern, Germany
reiner@hartenstein.de

Submission Guidelines:

Accepted and presented papers will be published in IEEE Xplore®. All manuscripts will be reviewed by at least three members of the program committee. Submissions should be a complete manuscript of novel unpublished work (not to exceed 8 pages of single spaced text, including figures and tables) or, in special cases, may be a summary of relevant work. Submissions should be in pdf-format. Templates can be found at:
http://www.ieee.org/web/publications/pubservices/confpub/AuthorTools/conferenceTemplates.html
Authors should register and submit their pages or electronically through login at the EasyChair portal:
https://www.easychair.org/conferences/?conf=patmos13
To submit a proposal for a panel session, special session, industrial session, tutorial, a workshop, a demo, a PhD forum, or, if you have a birds of a feather (BOF) proposal, or, have questions, please contact the program chairs.

Topics of Interest

Authors are invited to submit manuscripts of original unpublished research. This year a focus is on **power-efficiency**. The topics of interest include, but are not limited to:

Reliability and Technology Variations

- Modeling and simulation in the presence of variability
- Variation-aware circuit design
- Reliability issues in nanoscale circuits
- Soft errors and radiation hardening
- Methods and Architectures for fault dependability
- Resilient hardware/software architectures
- Design for self adaptive circuits and systems
- Sensors for power, variability, temperature, and aging

Low Power and Thermal-aware Design

- Design techniques for thermal-aware and low power circuits and systems
- Power/thermal-aware synthesis and floorplanning
- Policies for power and thermal optimization
- Power/Thermal Estimation and Optimization
- Power/Thermal-aware architectures
- Hardware-software interaction for power/temperature minimization
- Energy-harvesting
- Low Power Systems: wireless sensor networks, mobile computing

Compilers, operating systems and runtime systems

- Power efficiency through parallelizing compilers or parallel programming
- Concepts for programming novel multi-core architectures
- Real-time system compilers, operating systems and run-time systems

FPGAs and GPU-based accelerators

- Novel accelerator-based architectures and architectural features
- High-Level Abstractions and CAD tools for using accelerators
- Neuro-Inspired Accelerators for Computing
- Customized processor instruction sets
- Compilers optimizing for dynamically reconfigurable processor arrays (DRPAs)
- Case studies and challenges on DRPAs and accelerators

Power-efficient High-performance ICT and Data Centers

- Supercomputing: compilers, operating systems, run time systems
- Hardware-software interaction for low power high-performance
- Modeling and analysis of energy costs for ICT subsystems and infrastructures
- Power analysis for data centers, supercomputers, communication networks
- Cross layer approaches and new paradigms for power efficiency in ICT
- Power-efficient I/O interfaces and NoC design
- Low power high performance in extreme scale supercomputing
- Heterogeneous HPC by new storage technologies
- Case studies: test cases, or design study challenges on data stations or supercomputers

Application-specific power efficiency by algorithmic and analytic efforts

- Banking, financial modeling and financial database acceleration
- Social networks, games, entertainment, ambient intelligence, ubiquitous and wearable computing
- Bioinformatics, bio-inspired, medical, and genetics systems and life sciences
- Physics and astronomy, weather prediction, oil and gas exploration, and more
- Security systems, cryptography, object recognition and tracking, global navigation satellite systems
- Audio/video, imaging, smart cameras, PDAs, smart image sensors, Reconfigurable Video Coding (RVC), etc. Aerospace, avionics, automotive and railway, and many other application areas

Case studies

- ICT, wireless sensor networks, wireless health, green computing, ultra low-power embedded systems, displays
- Examples, studies or challenges presenting innovative solutions for thermal and power efficiency
- Studies and experiences in using Azido
- Studies about power efficiency in extreme scale supercomputing projects
- Studies on energy efficiency by paradigm shift, by heterogeneous solutions or new storage technologies
- Case Studies on power efficiency of data stations

New directions in CS Education

- Roadmap of reconfigurable computing: compiled accelerators, ASICs and ASIPs
- New concepts in teaching, in tutorials, novel curricula and laboratories
- Industry and academic collaborative programs
- Design techniques for thermal and low power circuits and systems at all levels of abstraction