



Call for Papers

Extended Deadline: June 7th, 2013

4th European Workshop on CMOS Variability

Karlsruhe, Germany, September 9-11, 2013

<http://www.itiv.kit.edu/patmos-vari2013/>



VARI 2013 is the **4th European Workshop on CMOS Variability**. The increasing variability in CMOS transistor characteristics, as well as its sensitivity to environmental variations has become a major challenge to scaling and integration. This leads to major changes in the way that future integrated circuits and systems are designed. Strong links must be established between circuit design, system design and device technology.

The VARI workshop answers to the need to have an **European event on variability in CMOS technology** development and circuit design, where industry and academia meet. VARI objective is to provide a forum to discuss and investigate the CMOS process and environmental variability issues in methodologies and tools for the design of current and upcoming generations of integrated circuits and systems. The technical program will focus on performance and power consumption as well as architectural aspects like adaptability or resilience, with particular emphasis on modeling, design, characterization, analysis and optimization in respect to variability. Digital, Analog, Mixed Signal and RF circuits are within VARI scope.

The venue of VARI 2013 will be the **Karlsruhe Institute of Technology (KIT)**, Germany. This year, **VARI 2013 will be collocated with PATMOS 2013**, a reference workshop on Power and timing modeling, optimization and simulation.

Committees

Co-General Chairs

Nadine Azemard, Nadine.Azemard@lirmm.fr
Joerg Henkel, henkel@ira.uka.de

Program Chair

Antonio Rubio, antonio.rubio@upc.edu
Marc Belleville, marc.belleville@cea.fr

Organizing Committee

Publicity Chair: Asen Asenov (*Glasgow Univ.*)
Industry Chair: Robin Wilson (*ST*)

Technical Program Committee

A. Asenov - Univ. Glasgow, UK
N. Azemard - LIRMM, France
E. Beigne - CEA-LETI, France
M. Belleville - CEA-LETI, France
R. Canal - UPC, Spain
J. Henkel - Univ. Karlsruhe, Germany
G. Jacquemod - Unice, France
A. Juge - ST Crolles, France
Si-Yu Liao - Univ. Glasgow, UK
P. Maurine - LIRMM, France
D. Pandini - ST Agrate, Italy
C. Piguet - CSEM, Switzerland
M. Poncino - Politecnico di Torino, Italy
A. Rubio - Univ. Catalunya, Spain
P. Scheiblin - CEA-LETI, France
D. Soudris - NTU Athens, Greece
R. Wilson - ST Crolles, France
P. Zuber, IMEC, Belgium
M. Zwolinski, Univ. of Southampton, UK

Papers are solicited on, but not limited to, the following topics:

Modeling and Simulation of Variations: from Physics to Circuits

Global, Systematic and Random process variations - Environmental variations (Power supply, Temperature, Electromagnetic Interferences, Ions or Electro-magnetic radiations) - Aging

Digital and Analog Design tools and Methodologies for Variability

Multi-Corners approaches including margining, Statistical approaches
Tools for variability at design, layout and post-layout levels

Measurements sensors and actuators for Digital and Analog

Process sensors, Temperature sensors, Direct and Indirect Performance sensors, Power and Energy sensors, Power supply and voltage droop sensors, Timing slacks and faults sensors, Multi-sensors fusion.

Global and Local Voltage scaling, Current biasing, Body biasing, Frequency scaling, Delay Tuning

Compensation at Digital or Analog Circuit Design Level

New digital & analog building blocks with enhanced robustness, Design centering, Operating point tracking, Asynchronous design, desynchronization techniques, Clock tree resynchronization

Compensation at Digital or Analog Layout Level

Regular layout, Restricted Design Rules, Optical Proximity Corrections, Design For Manufacturability

Compensation at Digital, Mixed or Analog architectural Level

Compensation loops for performances tuning, Global or distributed, static or dynamic optimization, Tasks remapping according to hardware capabilities,

Prospective authors are invited to submit an A4 camera ready paper, no later than **June 7th, 2013**, including a 100-word abstract, figures and references, not exceeding 6 pages or 5000 words. Electronic submission is required and should follow the IEEE double column style, for the final publication. Submitted papers will be reviewed formally by several reviewers. Accepted/Invited papers will be included in the PATMOS-VARI conference proceedings.

Selected papers will be included in a special issue of **The Journal of Low Power Electronics (JOLPE)**. Student Papers presented at the conference will be considered for the **Best Student Paper Award**. The award delivery will take place at the closing session of the workshop.



UNIVERSITAT POLITÈCNICA
DE CATALUNYA
BARCELONATECH

